Circuit Design in Advanced CMOS Technologies: How to Design with Lower Supply Voltages

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Technology scaling brings lower supply voltages. For advanced CMOS technology nodes of 40nm and beyond, this leads to specific challenges. In particular, analog circuits require specialized design approaches and innovative techniques. Maintaining high precision with reduced available signal swing while keeping energy consumption within reasonable bounds has presented challenges for many circuit designers. Increased technological variability and leakage only make this worse.

This short course provides an overview of the challenges and solutions of modern circuit design in advanced technologies with low supply voltage. The course will start with a system overview of the problem. Then, several types of circuits will be discussed. General analog and mixed-mode building blocks, A/D converters and RF components each are the subject of a separate talk.

A Roadmap to Lower Supply Voltages – A System Perspective

Jan Rabaey, University of California, Berkeley, CA

A novel class of devices that broadly fall under the rubrics of “Internet-of-things” and “wearable” may soon upend the unprecedented growth in mobile devices that we have witnessed over the past decades. For these devices to be viable, however, a continuous reduction in energy-per-operation is necessary. Unfortunately, the flattening of traditional semiconductor scaling means that only a small part of this reduction can be expected from technology advances. The good news is that one design parameter that has a huge impact on energy consumption - the supply voltage - is still substantially above the fundamental limits (at least for digital circuits). Hence this leaves ample room for innovative design techniques to explore further lowering of the supply voltage.

The largest hindrances to low supply voltages are leakage and uncertainty. The presence of leakage sets a minimum voltage (and energy) for digital operation in a given technology. Going beyond that requires an aggressive energy-management strategy. Addressing uncertainty (arising from process variations, temporal changes and data statistics) typically requires margins to ensure functionality and correctness. Hence techniques to minimize margining while guaranteeing correct operation are important. Both leakage and uncertainty management can be performed at many layers of the design hierarchy. In this lecture, we will present an overview of commonly used and emerging techniques, illustrated with industrial and academic examples.

About the presenter:

Jan Rabaey received his Ph.D. degree in applied sciences from the Katholieke Universiteit Leuven, Belgium. In 1987, he joined the faculty of the Electrical Engineering and Computer Science department of the University of California, Berkeley, where he now holds the Donald O. Pederson Distinguished Professorship. He is currently the scientific co-director of the Berkeley Wireless Research Center (BWRC), as well as the founding director of the Berkeley Ubiquitous SwarmLab.

Prof. Rabaey has made widely recognized contributions to a number of domains, including advanced wireless systems, sensor networks, configurable circuits and low-power design. His current interests include the conception and implementation of next-generation integrated wireless systems over a very broad range of applications, as well as exploring the interaction between the cyber and the biological world.

He is the recipient of a wide range of major awards, including the Semiconductor Industry Association (SIA) University Researcher Award. He is an IEEE Fellow and a member of the Royal Flemish Academy of Sciences and Arts of Belgium, and has been involved in a broad variety of start-up ventures.
Designing Ultra-Low-Voltage Analog and Mixed-Signal Circuits

Peter Kinget, Columbia University, New York, NY

This talk focuses on the challenges and solutions for designing analog circuits at supply voltages well below 1V. Fundamental limitations of the MOS transistor force us to rethink the most basic analog circuit configurations. At the same time, low-voltage operation offers new opportunities to use all four terminals of the transistor while the speed of nanoscale devices allows for different representations for analog signal information. The lecture discusses solutions for analog building blocks like amplifiers operating at ultra-low supply voltages, and how they can be used to build complete analog signal processing systems like filters, track-and-hold circuits or analog-to-digital converters.

About the presenter:
Peter R. Kinget received an engineering degree in electrical and mechanical engineering and the Ph.D. in electrical engineering from the Katholieke Universiteit Leuven, Belgium. He has worked in industrial research and development at Bell Laboratories, Broadcom, Cepat and Multilink before joining the faculty of the Department of Electrical Engineering, Columbia University, NY in 2002, where he is currently a Professor. He is also a consulting expert on patent litigation and a technical consultant to industry. His research interests are in analog, RF and power integrated circuits and the applications they enable in communications, sensing, and power management.

Dr. Kinget is a Fellow of the IEEE and is widely published. He is a co-recipient of several awards including the “First Prize” in the 2009 Vodafone Americas Foundation Wireless Innovation Challenge and the “2011 IEEE Communications Society Award for Advances in Communication.” He has been a “Distinguished Lecturer” for the IEEE Solid-State Circuits Society (SSCS), and an Associate Editor of the IEEE Journal of Solid State Circuits and the IEEE Transactions on Circuits and Systems II. He has served on the program committees of many of the major solid-state circuits conferences and currently is an elected member of the IEEE SSCS Adcom.

ADC Design in Scaled Technologies

Andrea Baschirotto, University of Milan-Bicocca, Milan, Italy

This talk focuses on recent developments in ADCs, which are one of the primary components in any mixed-signal integrated system.

The first part reviews the most relevant changes in MOS transistor behaviour when realized in scaled technologies (VDD reduction, gain reduction, VTH deviation, higher speed, etc.), focusing on how they affect ADC design.

After this, general trends in ADCs in the recent literature are analyzed, and the reported ADC implementations in the 32nm or below technologies are presented, looking at their innovative solutions, emphasizing the common trends and the difference between the several implementations.

About the presenter:
Andrea Baschirotto received his Ph.D. in electronics engineering in 1994 from Univ. Pavia. He is an Associate Professor at Univ. Milan-Bicocca, Italy. His main research interests are in the design of CMOS mixed analog/digital integrated circuits, in particular for low-power and/or high-speed signal processing. He participated in several research collaborations (also funded by National and European projects) and several collaboration between Universities and Industries. In 2010 he co-founded the start-up sparklingIC, of which he serves as CTO.

He has authored or co-authored more than 190 papers in international journals and presentations at international conferences, 6 book chapters, and holds 35 US patents. In addition, he has co-authored more than 120 papers within research collaborations on high-energy physics experiments.
Ultra-Low-Voltage RF Circuits and Transceivers

Hyunchol Shin, Kwangwoon University, Seoul, Korea

The continuing scaling of CMOS technology and the growing needs for single-cell battery operation drive the supply voltage of RF circuits toward the sub-1V region. As the supply voltage approaches only 2-3 times $V_{th}$, many traditional RF circuit topologies are becoming ineffective. Much effort has been spent rethinking the conventional circuit topologies and radio architectures for RF applications. This presentation focuses on the design issues and recent progress in transceiver architectures and building blocks to meet the sub-1V challenge.

The first part reviews several sub-1V design techniques that can be applied to many RF circuits. The second part covers the receiver and its key building blocks (LNA and mixer) discussing design fundamentals, advanced circuit topologies, and recent implementation examples for sub-1V operation. The third part covers the most power-hungry parts in RF transceivers, namely the VCO, frequency divider, and PLL synthesizer. The presentation concludes with interesting aspects and opportunities that are yet to come.

About the presenter:

Hyunchol Shin received the Ph.D. degree in electrical engineering from KAIST, Korea in 1998. After his Ph.D., he had gained professional experience at several institutions and companies, such as Samsung Electronics, Korea, University of California, Los Angeles, CA, Qualcomm, San Diego, CA, all working on RF/analog circuit design for wireless communications. Since 2003, he has been with Kwangwoon University, Seoul, Korea, where he is currently a Professor. From 2010 to 2011, he took a sabbatical leave at Qualcomm Corporate R&D, San Diego, CA. His research focuses on CMOS RF/analog/microwave circuits and PLL frequency synthesizers.

Prof. Shin has (co)authored over 70 journal and conference papers and holds 30 patents in the field of RF/analog circuit design. He is a Senior Member of the IEEE, and has served on the technical program committees of several IEEE conferences such as ISSCC, A-SSCC, MWSCAS, RFIT, ISOCC, and IWS.